# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/13/8087
Dated 06 Sep 2013

**M24C08, 8-Kbit serial I2C Bus EEPROM, Industrial grade,**

**Redesign and upgrade to the CMOSF8H+ process technology**

### Table 1. Change Implementation Schedule

| | |
|---|---|
| Forecasted implementation date for change | 30-Aug-2013 |
| Forecasted availability date of samples for customer | 16-Sep-2013 |
| Forecasted date for **STMicroelectronics** change Qualification Plan results availability | 01-Oct-2013 |
| Estimated date of changed product first shipment | 06-Dec-2013 |

### Table 2. Change Identification

| | |
|---|---|
| Product Identification (Product Family/Commercial Product) | M24C08 products family / Industrial grade |
| Type of change | Waferfab technology change |
| Reason for change | Line up to state-of-the-art of process |
| Description of the change | Redesign and upgrade to the new CMOSF8H+ process technology. |
| Change Product Identification | Process Technology identifier "T" for CMOSF8H+ |
| Manufacturing Location(s) | |

**Table 3. List of Attachments**

| Customer Part numbers list | |
| --- | --- |
| Qualification Plan results | |

- - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

| Customer Acknowledgement of Receipt | PCN MMS-MMY/13/8087 |
| --- | --- |
| Please sign and return to STMicroelectronics Sales Office | Dated 06 Sep 2013 |
| ☐ Qualification Plan Denied | Name: |
| ☐ Qualification Plan Approved | Title: |
| | Company: |
| ☐ Change Denied | Date: |
| ☐ Change Approved | Signature: |

Remark

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# DOCUMENT APPROVAL

| Name | Function |
| --- | --- |
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| Rodrigues, Benoit | Product Manager |
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# PRODUCT / PROCESS CHANGE NOTIFICATION

## M24C08, 8-Kbit serial I2C Bus EEPROM, Industrial grade
## Redesign and upgrade to the CMOSF8H+ process technology

**What is the change?**

The **M24C08**, 8-Kbit serial I²C bus EEPROM product family, industrial grade, currently produced using the CMOSF6SP 36% process technology at ST Ang Mo Kio (Singapore) 6" wafer diffusion plant or at GLOBALFOUNDRIES (Singapore) 8" wafer diffusion plant, has been **redesigned** and will be **upgraded** to the **CMOSF8H+** process technology at **ST Rousset** (France) 8" wafer diffusion plant.

The CMOSF8H+ is already qualified and in full production for M24C01, M24C02, M24C04 and M24C16.

This upgraded version in CMOSF8H+ allows offering:

- **1.7 V** / 5.5 V ("**-F**") Vcc range over industrial temperature range -40 / +85°C
- **Enhanced cycling** and **data retention** performances:
  - 4 million cycles
  - 200 years data retention

The new M24C08 in CMOSF8H+ version are functionally compatible with the current CMOSF6SP 36% version as per datasheet rev. 1 – December 2012, attached.

The new M24C08 will be described in datasheet with following differences versus previous datasheet rev. 1:

- DC characteristic:
- $I_{CC1}$ standby supply current:
  - Max 2 µA at $V_{CC}$ = 2.5 V
  - Max 3 µA at $V_{CC}$ = 5.5 V

- $I_{CC}$ supply current (Read):
  - Max 1 mA at $V_{CC}$ = 1.8 V

- Absolute maximum rating: $V_{ESD}$ electrostatic pulse Human Body model:
  - Max 3000 V

Concurrent to this change, the SO8N, TSSOP8 and UFDFPN8 packages will use 0.8 mil Copper wire (as used on M24C01, M24C02, M24C04, M24C16 in CMOSF8H+).

**Why?**

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M24C08 in the new CMOSF8H+ process technology will increase the production capacity throughput and consequently improve the service to our customers.

**When?**
The production of the upgraded M24C08 with the new CMOSF8H+ will ramp up from October 2013 and shipments can start from November 2013 onward (or earlier upon customer approval).

**How will the change be qualified?**
The new version of the M24C08 in CMOSF8H+ will be qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability. The CMOSF8H+ Process Technology is already qualified on the M24C16.

The **Qualification Plan QPMMY1233** is available and included inside this document.

**What is the impact of the change?**

**- Form:** Marking change (see **Device marking** paragraph)

**- Fit:** No change

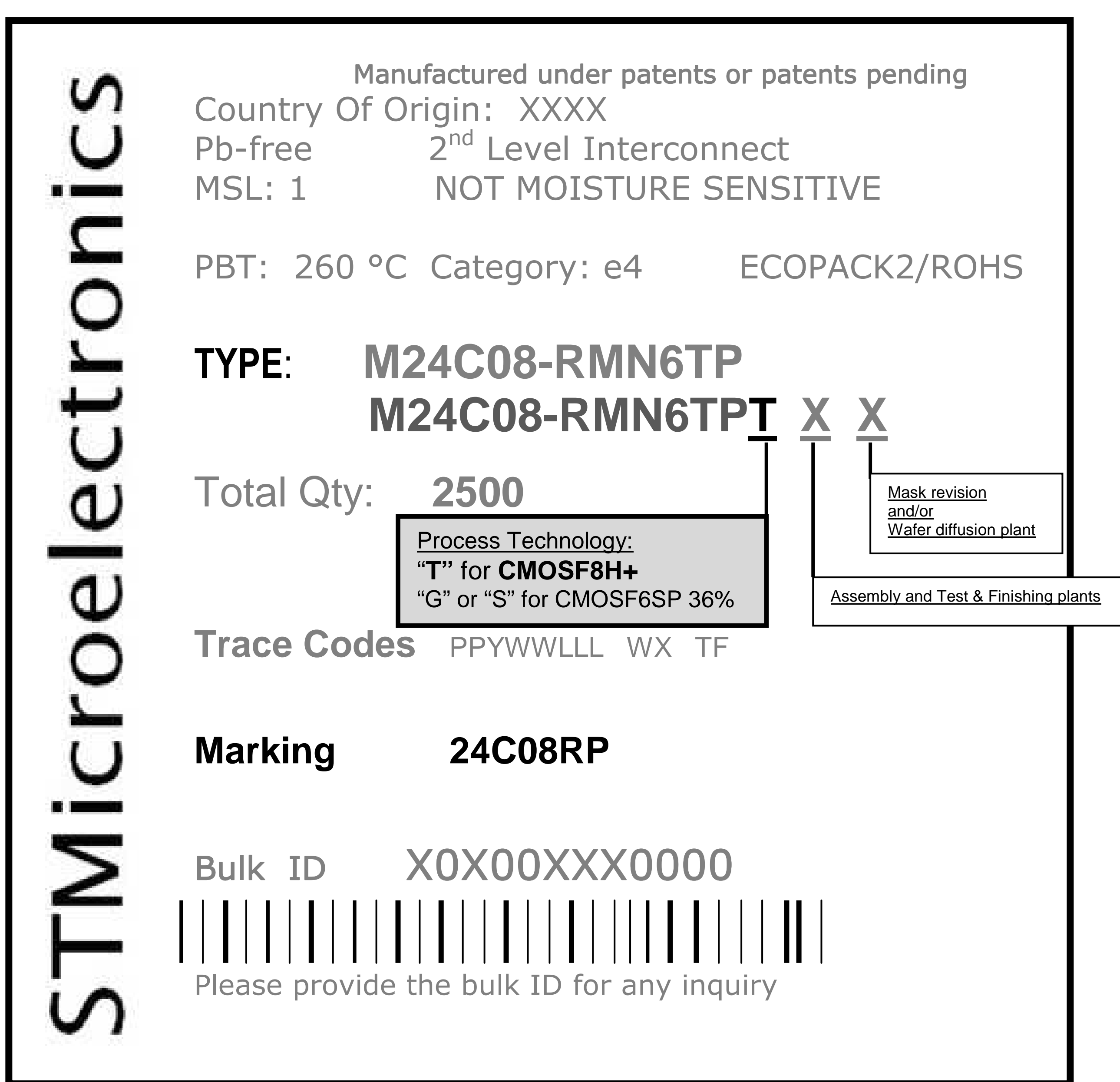
**- Function:**
- Change on DC characteristic $I_{CC1}$ **standby supply current &** $I_{CC}$ **supply current (Read)**
- Change on Absolute maximum rating $V_{ESD}$ **HBM**

## How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is "**T**" for the **upgraded version** in **CMOSF8H+**, this identifier being "G" or "S" for the current version in CMOSF6SP 36%.

➔ *Example for M24C08-RMN6TP*



## How can the change be seen?

## ***- DEVICE MARKING***

For the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit "T" for **process technology** identifier is "**T**" for the **upgraded version** in **CMOSF8H+**, this identifier being "Q" or "$" for current versions.

| | **Upgraded CMOSF8H+ (ST Rousset)** | Current CMOSF6SP 36% **(ST Ang Mo Kio)** | Current CMOSF6SP 36% **(GLOBALFOUNDRIES)** |
|---|---|---|---|
| **SO8N**<br>Example:<br>M24C08-RMN6TP | | | |





For the **TSSOP8** package, the difference is visible inside the product name where the last digit is "**T**" for the **upgraded version** in **CMOSF8H+**, this digit being "P" for current versions.

| | **Upgraded CMOSF8H+ (ST Rousset)** | Current CMOSF6SP 36% **(ST Ang Mo Kio) or GLOBALFOUNDRIES** |
|---|---|---|
| **TSSOP8**<br>Example:<br>M24C08-RDW6TP | | |




For the **UFDFPN8** package, the difference is visible inside the product name.
Example for M24C08-RMC6TG: **upgraded version** in **CMOSF8H+** is **4CRT**, current version is 408R.

| | **Upgraded CMOSF8H+ (ST Rousset)** | Current CMOSF6SP 36% **(ST Ang Mo Kio) or GLOBALFOUNDRIES** |
|---|---|---|
| **UFDFPN8**<br>Example:<br>M24C08-RMC6TG | O 4**CRT**<br>*PYWW* | O 4**08R**<br>*PYWW* |

## Appendix A- Product Change Information

| **Product family / Commercial products:** | M24C08 products family / Industrial grade |
|---|---|
| **Customer(s):** | All |
| **Type of change:** | Wafer fab & process technology change |
| **Reason for the change:** | Line up to state-of-the-art of process |
| **Description of the change:** | Redesign and upgrade to the new CMOSF8H+ Process technology. |
| **Forecast date of the change: (Notification to customer)** | Week **35** / 2013 |
| **Forecast date of Qualification samples availability for customer(s):** | Week **38** / 2013 |
| **Forecast date for the internal STMicroelectronics change, Qualification Report availability:** | The **Qualification Report QRMMY1233** will be available Week 40 / 2013. |
| **Marking to identify the changed product:** | Process Technology identifier "**T**" for CMOSF8H+ |
| **Description of the qualification program**: | Standard ST Microelectronics Corporate Procedures for Quality and Reliability |
| **Product Line(s) and/or Part Number(s):** | See Appendix B |
| **Manufacturing location:** | Rousset 8 inch wafer fab |
| **Estimated date of first shipment:** | Week **48** / 2013 |

## Appendix B: Concerned Commercial Part Numbers:

| Commercial Part Numbers | Package |
|---|---|
| M24C08-FMC5TG | UFDFPN8 |
| M24C08-RDW6TP | TSSOP8 |
| M24C08-RMC6TG | UFDFPN8 |
| M24C08-RMN6TP | SO8N |
| M24C08-WDW6TP | TSSOP8 |
| M24C08-WMN6P | SO8N |
| M24C08-WMN6TP | SO8N |

(*) Following product line rationalization, we recommend customer to use **–R** version (1.8 V – 5.5 V) when –W (2.5 V – 5.5 V) is used.
For instance, **M24C08-RMN6TP should be preferred** to M24C08-WMN6TP.

## Appendix C: Qualification Plan:

**See following pages**

# M24C08 Redesign and Upgrade to the CMOSF8H+ process technology Qualification Plan QPMMY1233 (1/4)



- The new version of the M24C08 in CMOSF8H+ will be qualified using the standard STMicroelectronics corporate procedures for quality and reliability.
- The CMOSF8H+ process technology has been qualified on 3 lots using the driver product M24C16 (refer to qualification report QRMMY1126).
- The new M24C08 is designed with the same architecture and technology as the driver product M24C16. Qualification of the new M24C08 benefits of the family approach (1 lot).

ST Restricted

# M24C08 Redesign and Upgrade to the CMOSF8H+ process technology Qualification Plan QPMMY1233 (2/4)



- The product vehicles used for the die qualification are presented in *Table 1*.

**Table 1. Product vehicles used for die qualification**

| Product | Silicon process technology | Wafer fabrication location | Package description | Assembly plant location |
|---|---|---|---|---|
| M24C16 | CMOSF8H+ | ST Rousset 8" | CDIP8 | Engineering assy (1) |
| M24C08 (2) | CMOSF8H+ | ST Rousset 8" | CDIP8 | Engineering assy (1) |

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C08 benefits of the family approach (1 lot).

- The package qualifications were mainly obtained by similarity. The product vehicles used for package qualification are presented in *Table 2*.

**Table 2. Product vehicles used for package qualification**

| Product | Silicon process technology | Wafer fabrication location | Package description | Assembly plant location |
|---|---|---|---|---|
| M24C16 (1) | CMOSF8H+ | ST Rousset 8" | SO8N | ST Shenzhen / Subcon Amkor |
| | | | TSSOP8 | ST Shenzhen / Subcon Amkor |
| | | | UFDFPN8 (MLP8) 2 x 3 mm | ST Calamba / Subcon Amkor |

1. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24C16 are applicable to M24C08.

# M24C08 Redesign and Upgrade to the CMOSF8H+ process technology Qualification Plan QPMMY1233 (3/4)



- The reliability test plan related to the new M24C08 is presented as follows :

| Test | Test short description | | | | | |
|---|---|---|---|---|---|---|
| | **Method** | **Conditions** | **Sample size / lots** | **No. of lots** | **Duration** | **Acceptance Criteria** |
| **EDR** | **High temperature operating life after endurance** | | | | | |
| | AEC-Q100-005 | 1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V | 80 | 1 | 1008 hrs | 0/80 |
| | **Data retention after endurance** | | | | | |
| | AEC-Q100-005 | 1 million E/W cycles at 25 °C then: HTSL 150 °C | 80 | 1 | 1008 hrs | 0/80 |
| **LTOL** | **Low temperature operating life** | | | | | |
| | JESD22-A108 | -40 °C, 6 V | 80 | 1 | 1008 hrs | 0/80 |
| **HTSL** | **High temperature storage life** | | | | | |
| | JESD22-A103 | Retention bake at 200 °C | 80 | 1 | 1008 hrs | 0/80 |
| **WEB** | **Program/erase endurance cycling + bake** | | | | | |
| | Internal spec. | 5 million cycles at 25 °C then: retention bake at 200 °C / 48 hrs | 80 | 1 | 5 million cycles / 48hrs | 0/80 |

# M24C08 Redesign and Upgrade to the CMOSF8H+ process technology Qualification Plan QPMMY1233 (4/4)



| Test | Test short description | | | | | |
|---|---|---|---|---|---|---|
| | **Method** | **Conditions** | **Sample size / lots** | **No. of lots** | **Duration** | **Acceptance Criteria** |
| **ESD HBM** | **Electrostatic discharge (human body model)** | | | | | |
| | AEC-Q100-002 JESD22-A114 | C = 100 pF, R = 1500 Ohms | 27 | 1 | N/A | PASS 3000 V |
| **ESD MM** | **Electrostatic discharge (machine model)** | | | | | |
| | AEC-Q100-003 JESD22-A115 | C = 200 pF, R = 0 Ohms | 12 | 1 | N/A | PASS 200 V |
| **ESD CDM** | **Electrostatic discharge (charge device model)** | | | | | |
| | AEC-Q100–011 JESD22-C101 | Field induced charging method | 18 | 1 | N/A | PASS 1500 V |
| **LU** | **Latch-up (current injection and over-voltage stress)** | | | | | |
| | AEC-Q100-004 JESD78B | At maximum operating temperature (150 °C) | 6 | 1 | N/A | Class II – Level A |

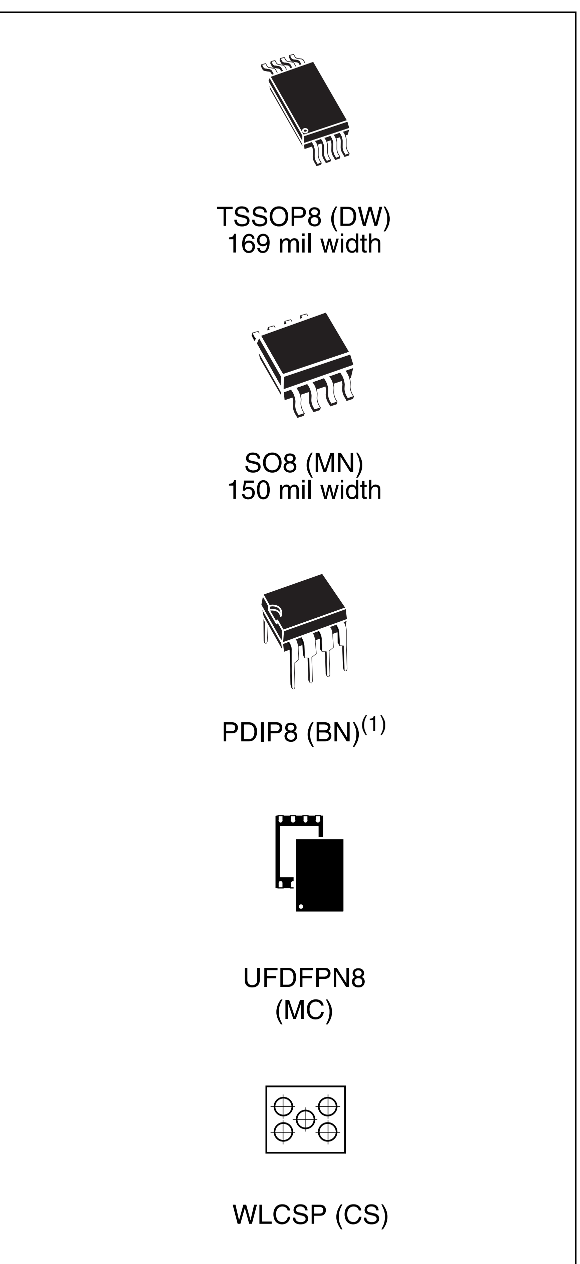
# M24C08-W M24C08-R M24C08-F

## 8-Kbit serial I²C bus EEPROM

**Datasheet — production data**

## Features

- Compatible with all $I^2C$ bus modes:
  - 400 kHz
  - 100 kHz
- Memory array:
  - 8 Kbit (1 Kbyte) of EEPROM
  - Page size: 16 bytes
- Single supply voltage:
  - M24C08-W: 2.5 V to 5.5 V
  - M24C08-R: 1.8 V to 5.5 V
  - M24C08-F: 1.7 V to 5.5 V
- Write:
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Operating temperature range: from -40 °C up to +85 °C
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 1 million Write cycles
- More than 40-year data retention
- Packages:
  - RoHS compliant and halogen-free (ECOPACK®)






This is information on a product in full production. www.st.com

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# 1 Description

The M24C08 is an 8-Kbit $I^2C$-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 1 K × 8 bits.

The M24C08-W can be accessed with a supply voltage from 2.5 V to 5.5 V, the M24C08-R can be accessed with a supply voltage from 1.8 V to 5.5 V, and the M24C08-F can be accessed with a supply voltage from 1.7 V to 5.5 V. All these devices operate with a clock frequency of 400 kHz (or less), over an ambient temperature range of -40 °C / +85 °C.

**Figure 1. Logic diagram**

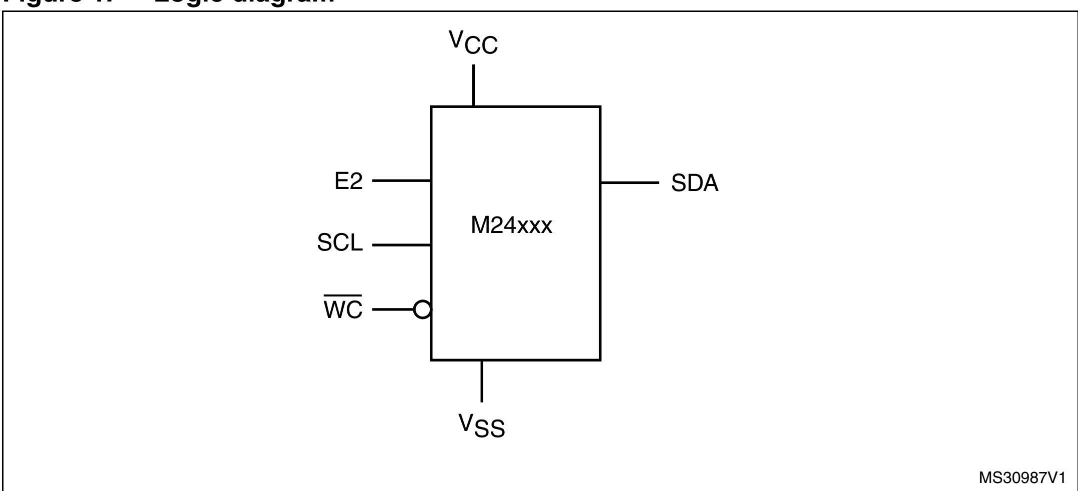
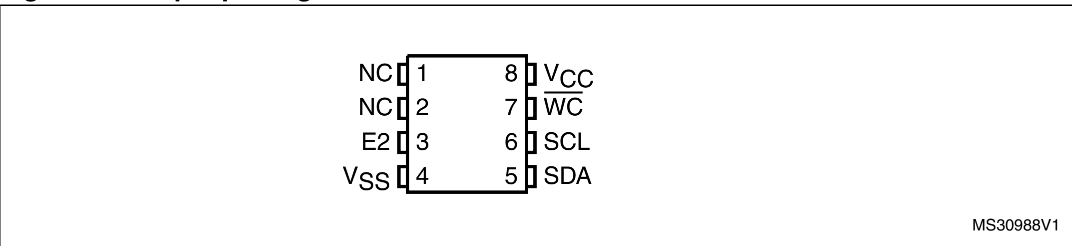



**Table 1. Signal names**

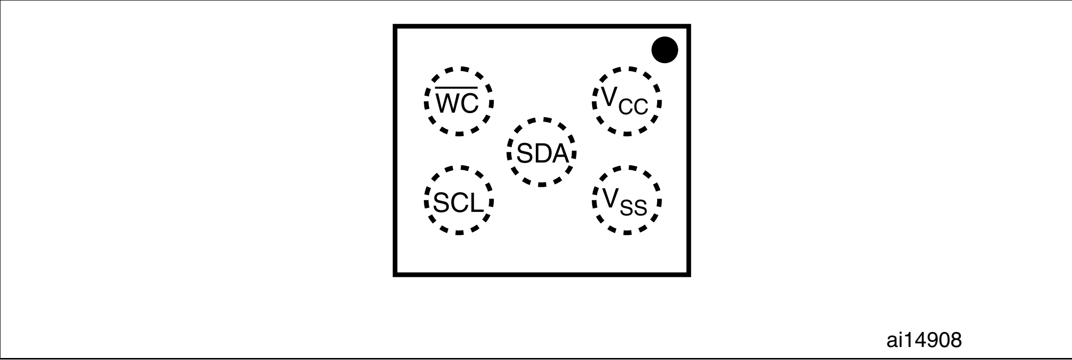
| Signal name | Function | Direction |
|---|---|---|
| E2 | Chip Enable | Input |
| SDA | Serial Data | I/O |
| SCL | Serial Clock | Input |
| $\overline{WC}$ | Write Control | Input |
| $V_{CC}$ | Supply voltage | |
| $V_{SS}$ | Ground | |

**Figure 2. 8-pin package connections**




1. NC: not connected.
2. See *Section 9: Package mechanical data* for package dimensions, and how to identify pin 1.

Figure 3. WLCSP connections (top view, marking side, with balls on the underside)




1. The E2 input is not connected to a ball, therefore E2 input is decoded as “0” (see also *Section 2.4: Write Control (WC)*).

**Caution:** As EEPROM cells lose their charge (and so their binary value) when exposed to ultra violet (UV) light, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UV light.

# 2 Signal description

## 2.1 Serial Clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

## 2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to $V_{CC}$ (*Figure 11* indicates how to calculate the value of the pull-up resistor).

## 2.3 Chip Enable (E2)

This input signal is used to set the value that is to be looked for on the bit b3 of the device select code. This input must be tied to $V_{CC}$ or $V_{SS}$, to establish the device select code as shown in *Table 2*. When not connected (left floating), this input is read as low (0).

## 2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. Write operations are enabled when Write Control ($\overline{WC}$) is either driven low or left floating.

When Write Control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

## 2.5 $V_{SS}$ (ground)

$V_{SS}$ is the reference for the $V_{CC}$ supply voltage.

## 2.6 Supply voltage ($V_{CC}$)

### 2.6.1 Operating supply voltage $V_{CC}$

Prior to selecting the memory and issuing instructions to it, a valid and stable $V_{CC}$ voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the $V_{CC}$ line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the $V_{CC}$/$V_{SS}$ package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle ($t_W$).

### 2.6.2 Power-up conditions

The $V_{CC}$ voltage has to rise continuously from 0 V up to the minimum $V_{CC}$ operating voltage (see Operating conditions in *Section 8: DC and AC parameters)* and the rise time must not vary faster than 1 V/µs.

### 2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until $V_{CC}$ has reached the internal reset threshold voltage. This threshold is lower than the minimum $V_{CC}$ operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When $V_{CC}$ passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until $V_{CC}$ reaches a valid and stable DC voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in $V_{CC}$), the device must not be accessed when $V_{CC}$ drops below $V_{CC}$(min). When $V_{CC}$ drops below the threshold voltage, the device stops responding to any instruction sent to it.

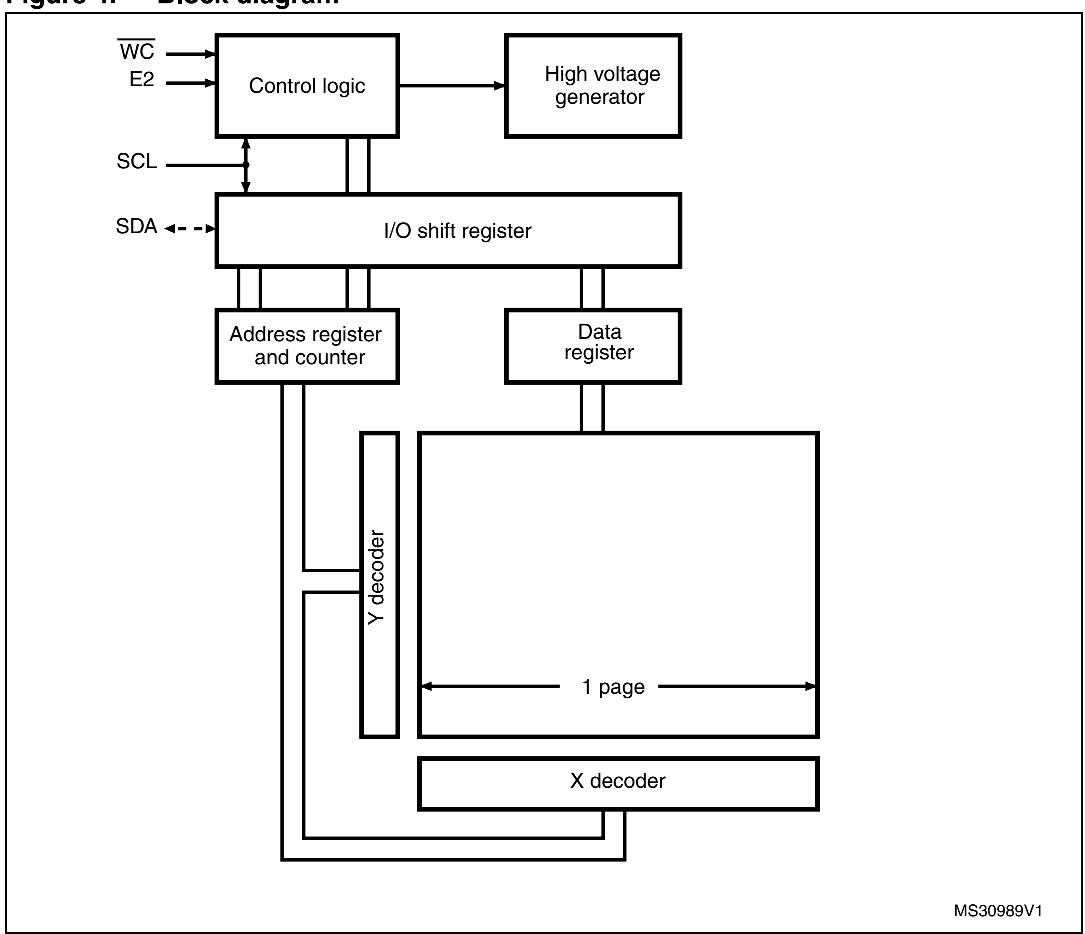
### 2.6.4 Power-down conditions

During power-down (continuous decrease in $V_{CC}$), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

# 3 Memory organization

The memory is organized as shown below.

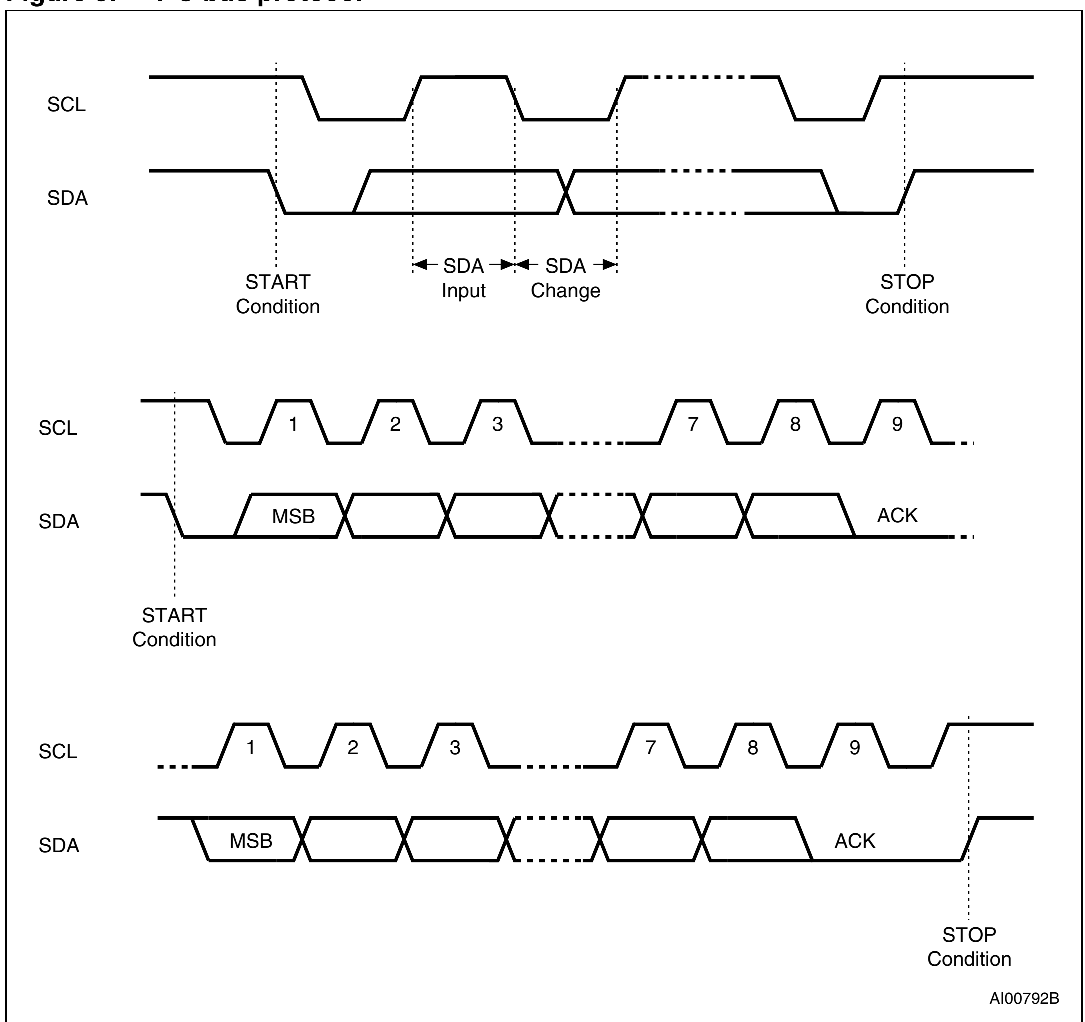
**Figure 4. Block diagram**



# 4 Device operation

The device supports the $I^2C$ protocol. This is summarized in *Figure 5*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

**Figure 5. $I^2C$ bus protocol**



## 4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

## 4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

## 4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

## 4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the $9^{th}$ clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

## 4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

**Table 2. Device select code**

| Device type identifier[1] | | | | Chip Enable address | | | R$\overline{W}$ |
|---|---|---|---|---|---|---|---|
| **b7** | **b6** | **b5** | **b4** | **b3** | **b2** | **b1** | **b0** |
| 1 | 0 | 1 | 0 | E2 | A9 | A8 | R$\overline{W}$ |

1. The most significant bit, b7, is sent first.

The 8th bit is the Read/$\overline{\text{Write}}$ bit (R$\overline{W}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

# 5 Instructions

## 5.1 Write operations

Following a Start condition the bus master sends a device select code with the $R/\overline{W}$ bit ($R\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 6*, and waits for the address byte. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

**Table 3. Address byte**

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| --- | --- | --- | --- | --- | --- | --- | --- |

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "$10^{th}$ bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle $t_W$ is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle ($t_W$), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in *Figure 7*.

### 5.1.1 Byte Write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 6*.

**Figure 6. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)**

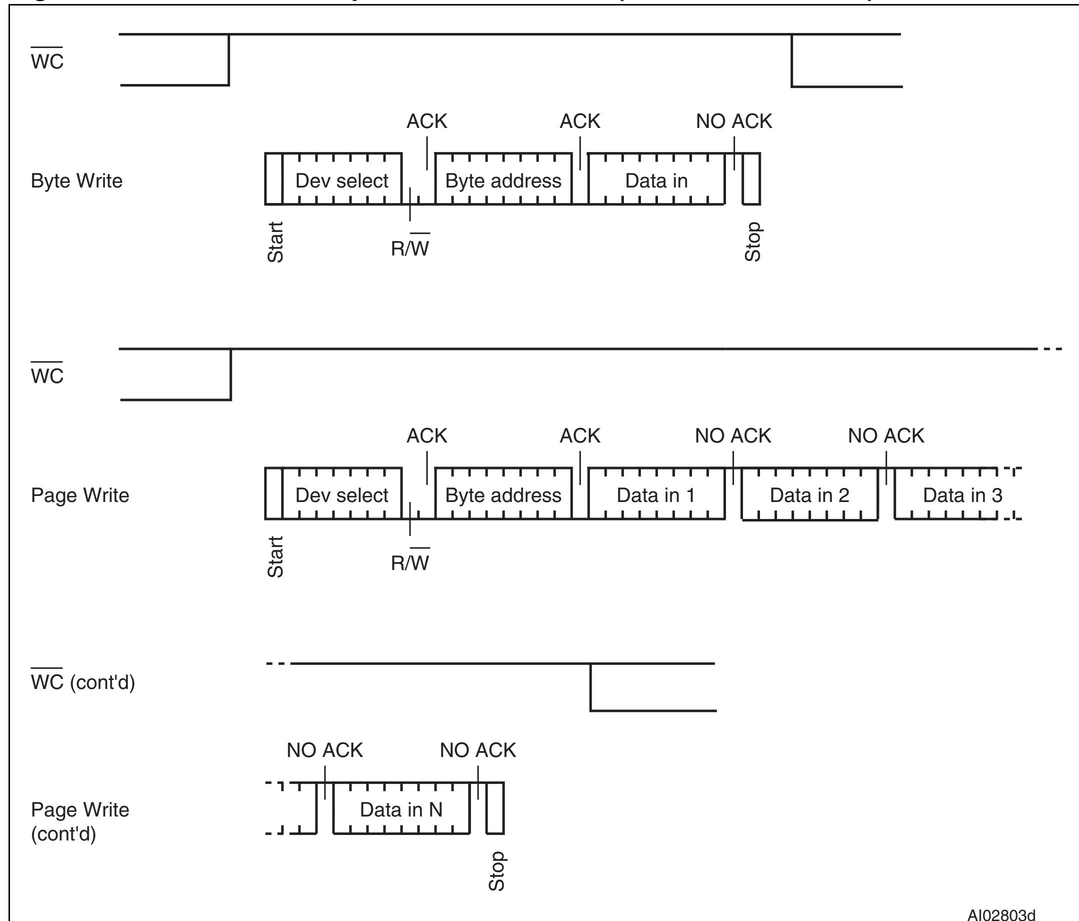
### 5.1.2 Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A9/A4, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If Write Control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 7*. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

**Figure 7. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)**



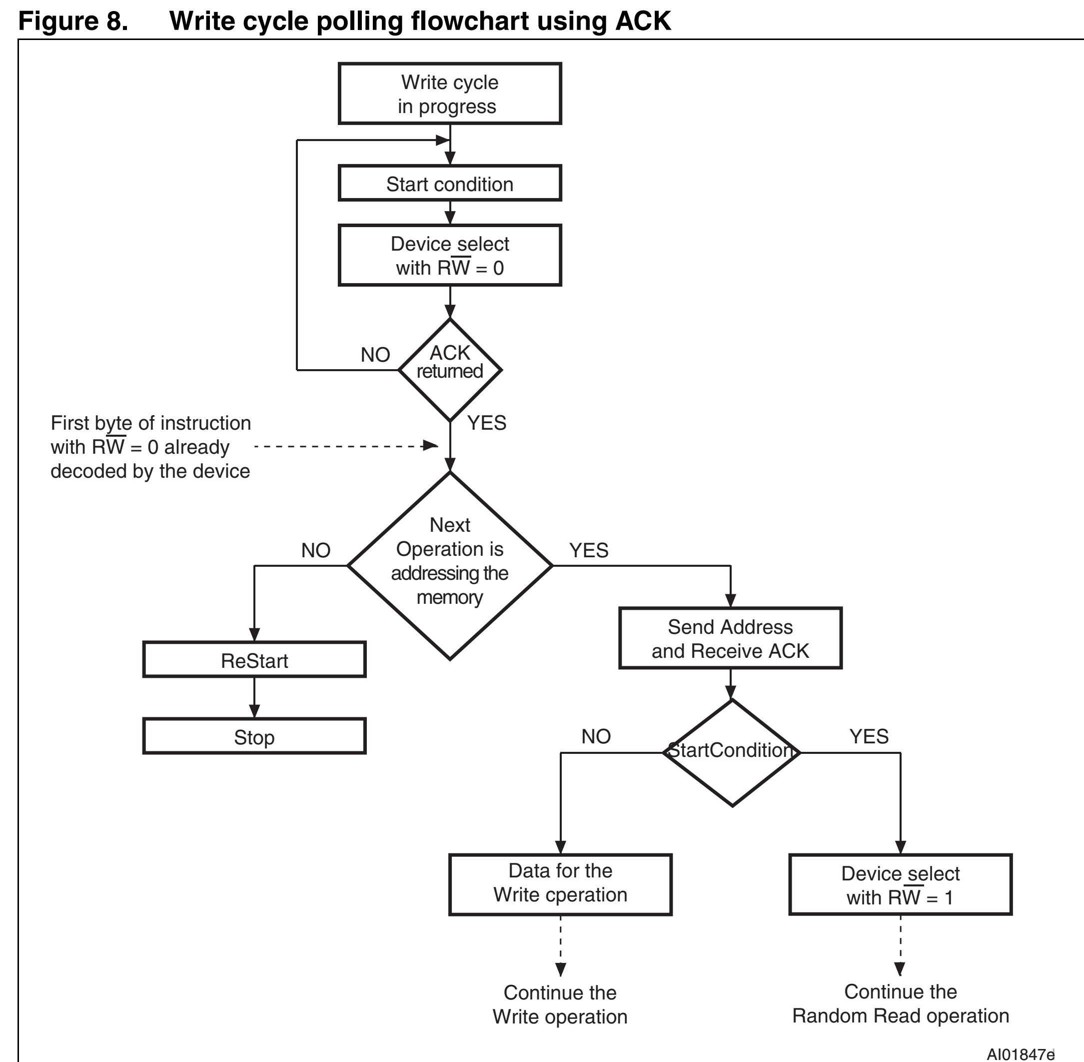
### 5.1.3 Minimizing Write delays by polling on ACK

The maximum Write time ($t_w$) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 8*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

**Figure 8. Write cycle polling flowchart using ACK**



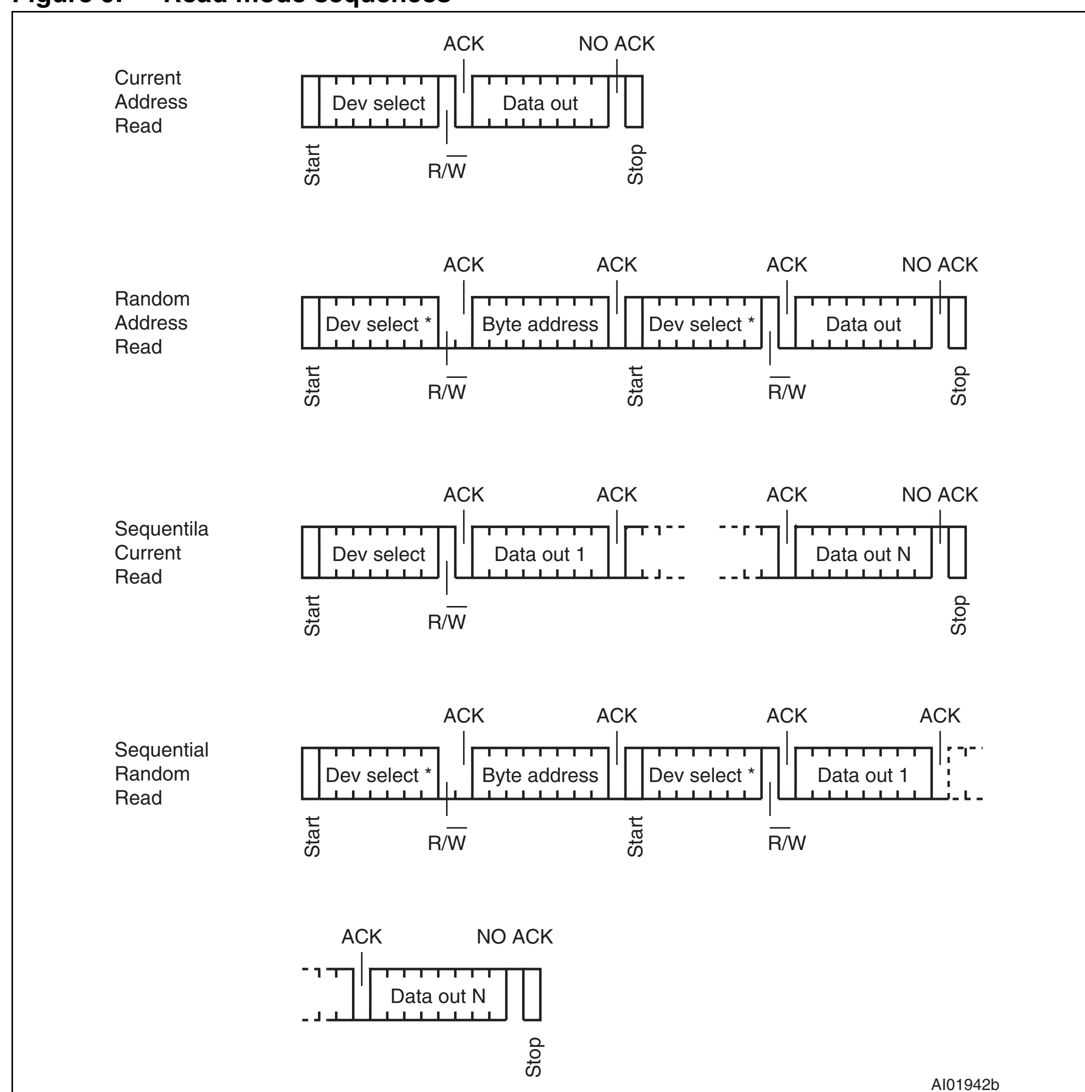
## 5.2 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

**Figure 9. Read mode sequences**



### 5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 9*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the $R\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

### 5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the $R/\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9*, *without* acknowledging the byte.

### 5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

# 6 Initial delivery state

The device is delivered with all the memory array bits and Identification page bits set to 1 (each byte contains FFh).

# 7 Maximum rating

Stressing the device outside the ratings listed in *Table 4* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| | Ambient operating temperature | –40 | 130 | °C |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |
| $T_{LEAD}$ | Lead temperature during soldering | see note[1] | | °C |
| | PDIP-specific lead temperature during soldering | - | 260[2] | °C |
| $I_{OL}$ | DC output current (SDA = 0) | - | 5 | mA |
| $V_{IO}$ | Input or output range | –0.50 | 6.5 | V |
| $V_{CC}$ | Supply voltage | –0.50 | 6.5 | V |
| $V_{ESD}$ | Electrostatic pulse (Human Body model)[3] | - | 4000 | V |

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. $T_{LEAD}$ max must not be applied for more than 10 s.
3. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω).

# 8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

**Table 5. Operating conditions (voltage range W)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.5 | 5.5 | V |
| $T_A$ | Ambient operating temperature | –40 | 85 | °C |
| $f_C$ | Operating clock frequency | - | 400 | kHz |

**Table 6. Operating conditions (voltage range R)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 1.8 | 5.5 | V |
| $T_A$ | Ambient operating temperature | –40 | 85 | °C |
| $f_C$ | Operating clock frequency | - | 400 | kHz |

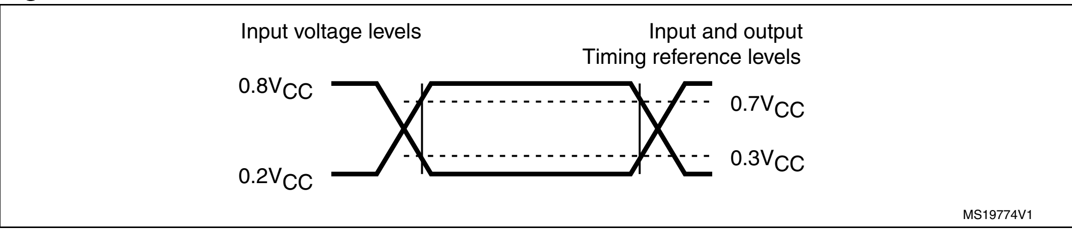
**Table 7. Operating conditions (voltage range F)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 1.7 | 5.5 | V |
| $T_A$ | Ambient operating temperature | –20 | 85 | °C |
| $f_C$ | Operating clock frequency | - | 400 | kHz |

**Table 8. AC measurement conditions**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{bus}$ | Load capacitance | 100 | | pF |
| | SCL input rise/fall time, SDA input fall time | - | 50 | ns |
| | Input levels | 0.2 $V_{CC}$ to 0.8 $V_{CC}$ | | V |
| | Input and output timing reference levels | 0.3 $V_{CC}$ to 0.7 $V_{CC}$ | | V |

**Figure 10. AC measurement I/O waveform**



### Table 9. Input parameters

| Symbol | Parameter[1] | Test condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance (SDA) | - | - | 8 | pF |
| $C_{IN}$ | Input capacitance (other pins) | - | - | 6 | pF |
| $Z_L$ | Input impedance ($\overline{WC}$) | $V_{IN} < 0.3\ V_{CC}$ | 15 | 70 | kΩ |
| $Z_H$ | | $V_{IN} > 0.7\ V_{CC}$ | 500 | - | kΩ |

1. Characterized only, not tested in production.

### Table 10. Memory cell data retention

| Parameter | Test condition | Min. | Unit |
|---|---|---|---|
| Data retention[1] | TA = 55 °C | 40 | Year |

1. The data retention behavior is checked in production. The 40-year limit is defined from characterization and qualification results.

### Table 11. DC characteristics (M24C08-W, device grade 6)

| Symbol | Parameter | Test conditions (in addition to those in *Table 5* and *Table 8*) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current (SCL, SDA, E2) | $V_{IN} = V_{SS}$ or $V_{CC}$, device in Standby mode | - | ± 2 | µA |
| $I_{LO}$ | Output leakage current | SDA in Hi-Z, external voltage applied on SDA: $V_{SS}$ or $V_{CC}$ | - | ± 2 | µA |
| $I_{CC}$ | Supply current (Read) | $V_{CC} = 5$ V, $f_c = 400$ kHz | - | 2[1] | mA |
| | | $V_{CC} = 2.5$ V, $f_c = 400$ kHz | - | 1 | mA |
| $I_{CC1}$ | Standby supply current | Device not selected[2], $V_{IN} = V_{SS}$ or $V_{CC}$, for 2.5 V < $V_{CC}$ < 5.5 V | - | 1 | µA |
| $V_{IL}$ | Input low voltage (SCL, SDA, $\overline{WC}$) | | –0.45 | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage (SCL, SDA, $\overline{WC}$) | | 0.7 $V_{CC}$ | $V_{CC}$ +1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL} = 2.1$ mA, $V_{CC} = 2.5$ V or<br>$I_{OL} = 3$ mA, $V_{CC} = 5.5$ V | - | 0.4 | V |

1. 2 mA for devices identified by process letter G or S.
2. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle $t_W$ ($t_W$ is triggered by the correct decoding of a Write instruction).

Table 12. DC characteristics (M24C08-R, device grade 6)

| Symbol | Parameter | Test conditions[1] (in addition to those in *Table 6* and *Table 8*) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current (E2, SCL, SDA) | $V_{IN} = V_{SS}$ or $V_{CC}$, device in Standby mode | - | ± 2 | µA |
| $I_{LO}$ | Output leakage current | SDA in Hi-Z, external voltage applied on SDA: $V_{SS}$ or $V_{CC}$ | - | ± 2 | µA |
| $I_{CC}$ | Supply current (Read) | $V_{CC}$ = 1.8 V, $f_c$= 400 kHz | - | 0.8 | mA |
| $I_{CC1}$ | Standby supply current | Device not selected[2], $V_{IN} = V_{SS}$ or $V_{CC}$, $V_{CC}$ = 1.8 V | - | 1 | µA |
| $V_{IL}$ | Input low voltage (SCL, SDA, $\overline{WC}$) | 2.5 V ≤ $V_{CC}$ | –0.45 | 0.3 $V_{CC}$ | V |
| | | 1.8 V ≤ $V_{CC}$ < 2.5 V | –0.45 | 0.25 $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage (SCL, SDA, $\overline{WC}$) | | 0.7 $V_{CC}$ | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 0.7 mA, $V_{CC}$ = 1.8 V | - | 0.2 | V |

1. If the application uses the voltage range R device with 2.5 V ≥ $V_{cc}$ < 5.5 V, please refer to *Table 11* instead of this table.
2. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle $t_W$ ($t_W$ is triggered by the correct decoding of a Write instruction).

Table 13. DC characteristics (M24C08-F, device )

| Symbol | Parameter | Test conditions[1] (in addition to those in *Table 7* and *Table 8*) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current (E2, SCL, SDA) | $V_{IN} = V_{SS}$ or $V_{CC}$, device in Standby mode | - | ± 2 | µA |
| $I_{LO}$ | Output leakage current | $V_{OUT} = V_{SS}$ or $V_{CC}$, SDA in Hi-Z | - | ± 2 | µA |
| $I_{CC}$ | Supply current (Read) | $V_{CC}$ = 1.7 V, $f_c$= 400 kHz | - | 0.8 | mA |
| $I_{CC1}$ | Standby supply current | Device not selected[2], $V_{IN} = V_{SS}$ or $V_{CC}$, $V_{CC}$ = 1.7 V | - | 1 | µA |
| $V_{IL}$ | Input low voltage (SCL, SDA, $\overline{WC}$) | 2.5 V ≤ $V_{CC}$ | –0.45 | 0.3 $V_{CC}$ | V |
| | | 1.7 V ≤ $V_{CC}$ < 2.5 V | –0.45 | 0.25 $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage (SCL, SDA, $\overline{WC}$) | | 0.7 $V_{CC}$ | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 0.7 mA, $V_{CC}$ = 1.7 V | - | 0.2 | V |

1. If the application uses the voltage range F device with 2.5 V ≥ $V_{cc}$ < 5.5 V, please refer to *Table 11* instead of this table.
2. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle $t_W$ ($t_W$ is triggered by the correct decoding of a Write instruction).

**Table 14. 400 kHz AC characteristics**

| Symbol | Alt. | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_C$ | $f_{SCL}$ | Clock frequency | - | 400 | kHz |
| $t_{CHCL}$ | $t_{HIGH}$ | Clock pulse width high | 600 | - | ns |
| $t_{CLCH}$ | $t_{LOW}$ | Clock pulse width low | 1300 | - | ns |
| $t_{QL1QL2}$(1) | $t_F$ | SDA (out) fall time | 20(2) | 300 | ns |
| $t_{XH1XH2}$ | $t_R$ | Input signal rise time | (3) | (3) | ns |
| $t_{XL1XL2}$ | $t_F$ | Input signal fall time | (3) | (3) | ns |
| $t_{DXCX}$ | $t_{SU:DAT}$ | Data in set up time | 100 | - | ns |
| $t_{CLDX}$ | $t_{HD:DAT}$ | Data in hold time | 0 | - | ns |
| $t_{CLQX}$(4) | $t_{DH}$ | Data out hold time | 100 | - | ns |
| $t_{CLQV}$(5) | $t_{AA}$ | Clock low to next data valid (access time) | - | 900 | ns |
| $t_{CHDL}$ | $t_{SU:STA}$ | Start condition setup time | 600 | - | ns |
| $t_{DLCL}$ | $t_{HD:STA}$ | Start condition hold time | 600 | - | ns |
| $t_{CHDH}$ | $t_{SU:STO}$ | Stop condition set up time | 600 | - | ns |
| $t_{DHDL}$ | $t_{BUF}$ | Time between Stop condition and next Start condition | 1300 | - | ns |
| $t_W$ | $t_{WR}$ | Write time | - | 5 | ms |
| $t_{NS}$(1) | | Pulse width ignored (input filter on SCL and SDA) - single glitch | - | 100 | ns |

1. Characterized only, not tested in production.
2. With $C_L$ = 10 pF.
3. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when $f_C$ < 400 kHz.
4. The min value for $t_{CLQX}$ (Data out hold time) of the M24xxx devices offers a safe timing to bridge the undefined region of the falling edge SCL.
5. $t_{CLQV}$ is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 $V_{CC}$ or 0.7 $V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 11*.

Table 15. 100 kHz AC characteristics ($I^2C$ Standard mode)(1)

| Symbol | Alt. | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_C$ | $f_{SCL}$ | Clock frequency | - | 100 | kHz |
| $t_{CHCL}$ | $t_{HIGH}$ | Clock pulse width high | 4 | - | µs |
| $t_{CLCH}$ | $t_{LOW}$ | Clock pulse width low | 4.7 | - | µs |
| $t_{XH1XH2}$ | $t_R$ | Input signal rise time | - | 1 | µs |
| $t_{XL1XL2}$ | $t_F$ | Input signal fall time | - | 300 | ns |
| $t_{QL1QL2}$(2) | $t_F$ | SDA fall time | - | 300 | ns |
| $t_{DXCX}$ | $t_{SU:DAT}$ | Data in setup time | 250 | - | ns |
| $t_{CLDX}$ | $t_{HD:DAT}$ | Data in hold time | 0 | - | ns |
| $t_{CLQX}$(3) | $t_{DH}$ | Data out hold time | 200 | - | ns |
| $t_{CLQV}$(4) | $t_{AA}$ | Clock low to next data valid (access time) | - | 3450 | ns |
| $t_{CHDL}$(5) | $t_{SU:STA}$ | Start condition setup time | 4.7 | - | µs |
| $t_{DLCL}$ | $t_{HD:STA}$ | Start condition hold time | 4 | - | µs |
| $t_{CHDH}$ | $t_{SU:STO}$ | Stop condition setup time | 4 | - | µs |
| $t_{DHDL}$ | $t_{BUF}$ | Time between Stop condition and next Start condition | 4.7 | - | µs |
| $t_W$ | $t_{WR}$ | Write time | - | 5 | ms |
| $t_{NS}$(2) | | Pulse width ignored (input filter on SCL and SDA), single glitch | - | 100 | ns |

1. Values recommended by the $I^2C$ bus Standard-mode specification for a robust design of the $I^2C$ bus application. Note that the M24xxx devices decode correctly faster timings as specified in *Table 14: 400 kHz AC characteristics*.
2. Characterized only.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. $t_{CLQV}$ is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 $V_{CC}$ or 0.7 $V_{CC}$, taking into account the Rbus × Cbus time constant specific to the end application.
5. For a reStart condition, or following a Write cycle.

**Figure 11. Maximum $R_{bus}$ value versus bus parasitic capacitance ($C_{bus}$) for an $I^2C$ bus at maximum frequency $f_C$ = 400 kHz**

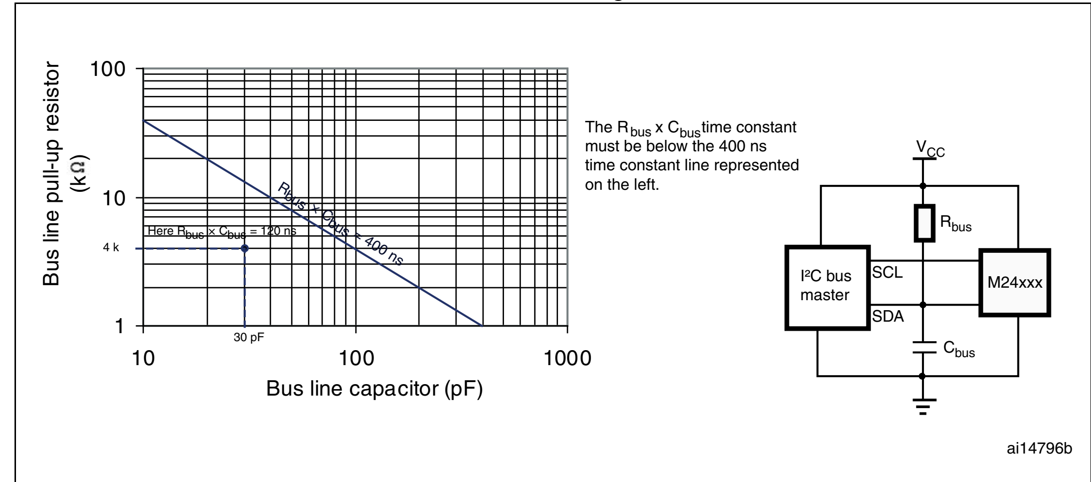
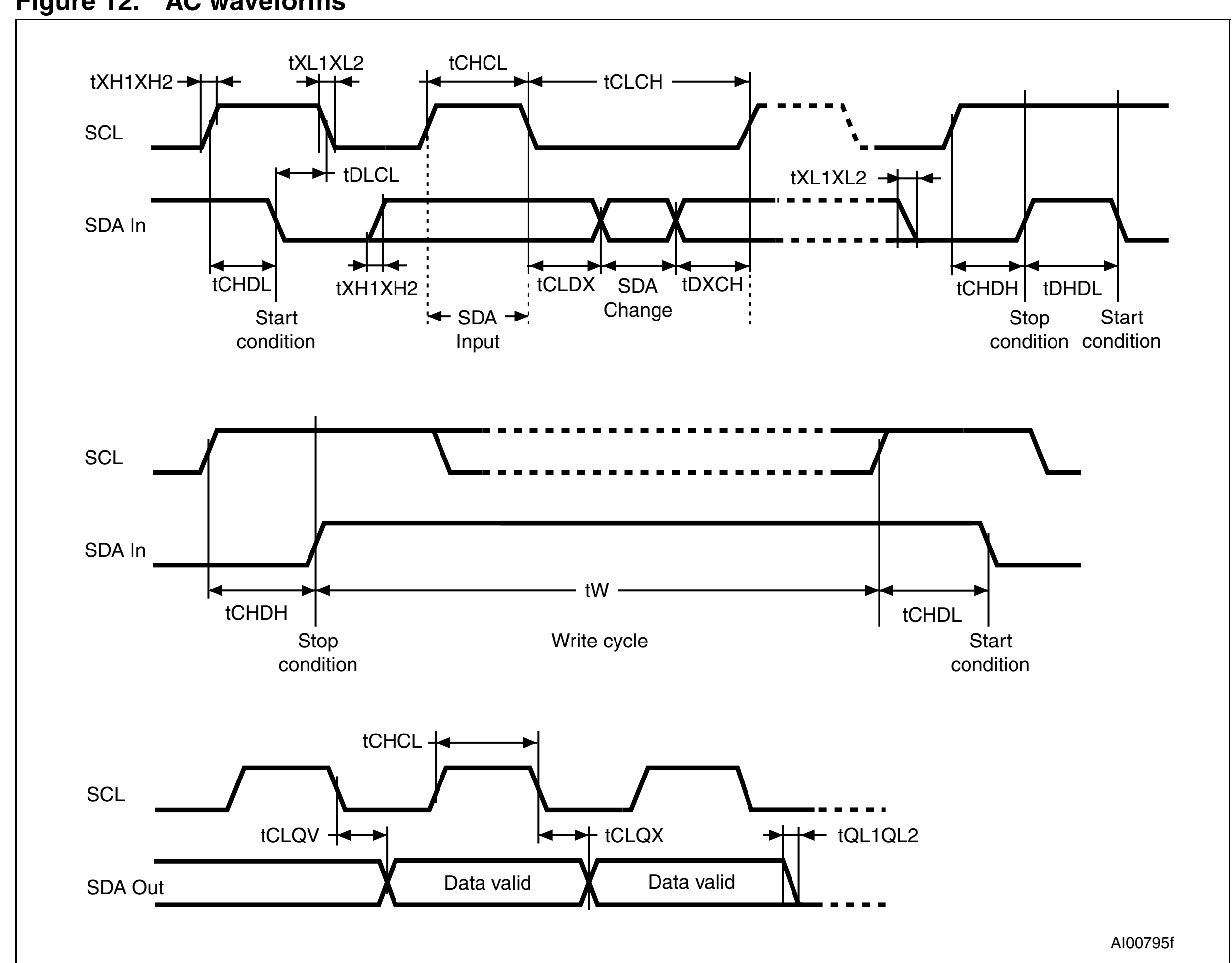


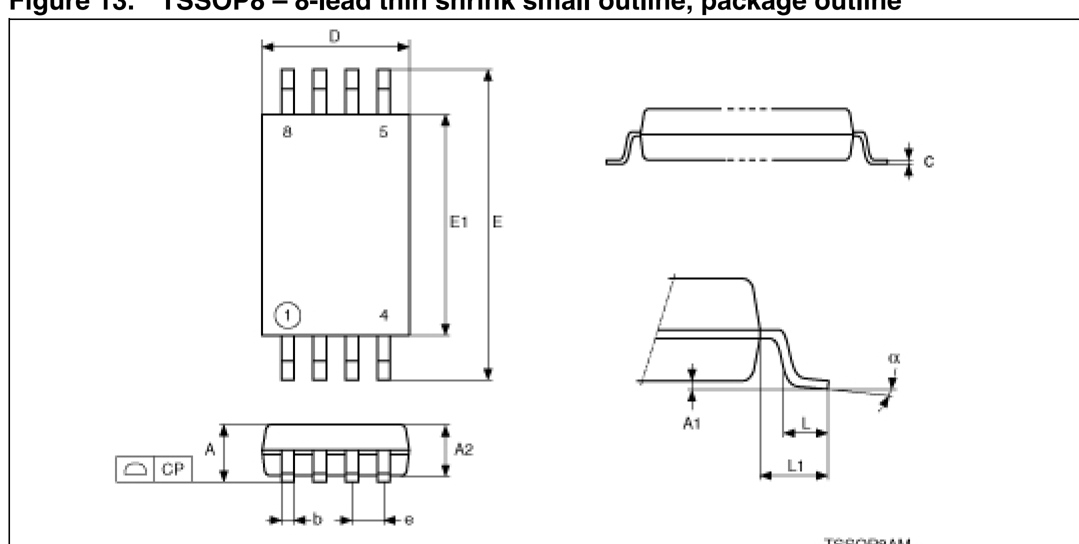
**Figure 12. AC waveforms**



# 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

**Figure 13. TSSOP8 – 8-lead thin shrink small outline, package outline**



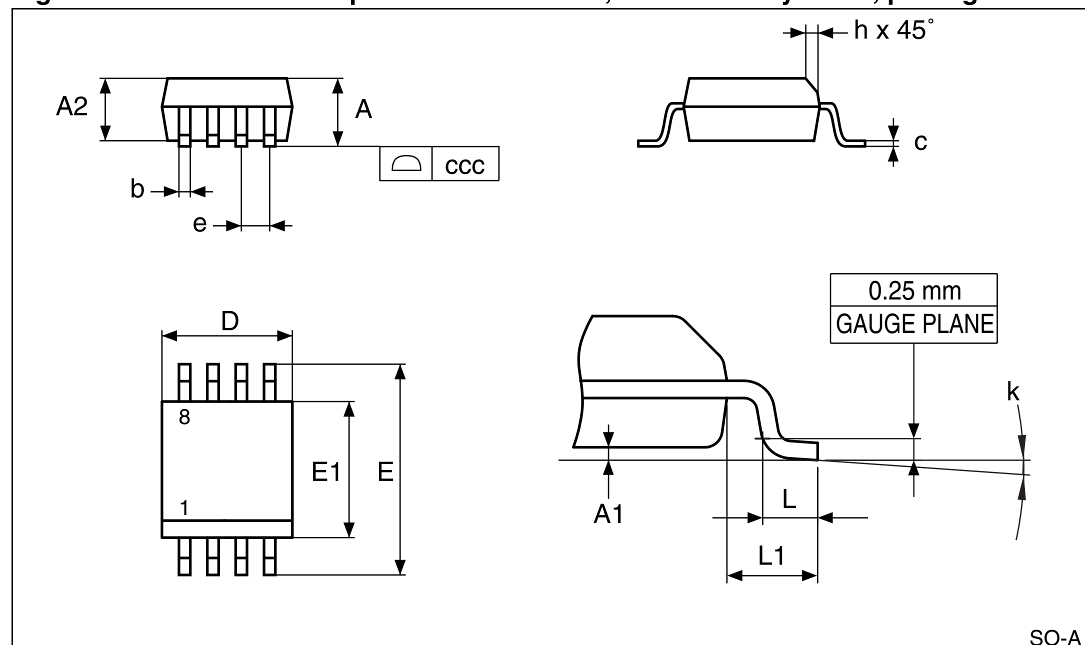

1. Drawing is not to scale.

**Table 16. TSSOP8 – 8-lead thin shrink small outline, package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | | 1.200 | | | 0.0472 |
| A1 | | 0.050 | 0.150 | | 0.0020 | 0.0059 |
| A2 | 1.000 | 0.800 | 1.050 | 0.0394 | 0.0315 | 0.0413 |
| b | | 0.190 | 0.300 | | 0.0075 | 0.0118 |
| c | | 0.090 | 0.200 | | 0.0035 | 0.0079 |
| CP | | | 0.100 | | | 0.0039 |
| D | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| e | 0.650 | | | 0.0256 | | |
| E | 6.400 | 6.200 | 6.600 | 0.2520 | 0.2441 | 0.2598 |
| E1 | 4.400 | 4.300 | 4.500 | 0.1732 | 0.1693 | 0.1772 |
| L | 0.600 | 0.450 | 0.750 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.000 | | | 0.0394 | | |
| α | | 0° | 8° | | 0° | 8° |

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 14. SO8N – 8-lead plastic small outline, 150 mils body width, package outline




1. Drawing is not to scale.

Table 17. SO8N – 8-lead plastic small outline, 150 mils body width, package data

| Symbol | millimeters | | | inches (1) | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.750 | | | 0.0689 |
| A1 | | 0.100 | 0.250 | | 0.0039 | 0.0098 |
| A2 | | 1.250 | | | 0.0492 | |
| b | | 0.280 | 0.480 | | 0.0110 | 0.0189 |
| c | | 0.170 | 0.230 | | 0.0067 | 0.0091 |
| ccc | | | 0.100 | | | 0.0039 |
| D | 4.900 | 4.800 | 5.000 | 0.1929 | 0.1890 | 0.1969 |
| E | 6.000 | 5.800 | 6.200 | 0.2362 | 0.2283 | 0.2441 |
| E1 | 3.900 | 3.800 | 4.000 | 0.1535 | 0.1496 | 0.1575 |
| e | 1.270 | | | 0.0500 | | |
| h | | 0.250 | 0.500 | | 0.0098 | 0.0197 |
| k | | 0° | 8° | | 0° | 8° |
| L | | 0.400 | 1.270 | | 0.0157 | 0.0500 |
| L1 | 1.040 | | | 0.0409 | | |

1. Values in inches are converted from mm and rounded to four decimal digits.

**Figure 15. PDIP8 – 8-pin plastic DIP, 0.25 mm lead frame, package outline**



1. Drawing is not to scale.
2. Not recommended for new designs.

**Table 18. PDIP8 – 8-pin plastic DIP, 0.25 mm lead frame, package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | | 5.33 | | | 0.2098 |
| A1 | | 0.38 | | | 0.0150 | |
| A2 | 3.30 | 2.92 | 4.95 | 0.1299 | 0.1150 | 0.1949 |
| b | 0.46 | 0.36 | 0.56 | 0.0181 | 0.0142 | 0.0220 |
| b2 | 1.52 | 1.14 | 1.78 | 0.0598 | 0.0449 | 0.0701 |
| c | 0.25 | 0.20 | 0.36 | 0.0098 | 0.0079 | 0.0142 |
| D | 9.27 | 9.02 | 10.16 | 0.3650 | 0.3551 | 0.4000 |
| E | 7.87 | 7.62 | 8.26 | 0.3098 | 0.3000 | 0.3252 |
| E1 | 6.35 | 6.10 | 7.11 | 0.2500 | 0.2402 | 0.2799 |
| e | 2.54 | – | – | 0.1000 | – | – |
| eA | 7.62 | – | – | 0.3000 | – | – |
| eB | | | 10.92 | | | 0.4299 |
| L | 3.30 | 2.92 | 3.81 | 0.1299 | 0.1150 | 0.1500 |

1. Values in inches are converted from mm and rounded to four decimal digits.

**Figure 16. UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat no lead, package outline**



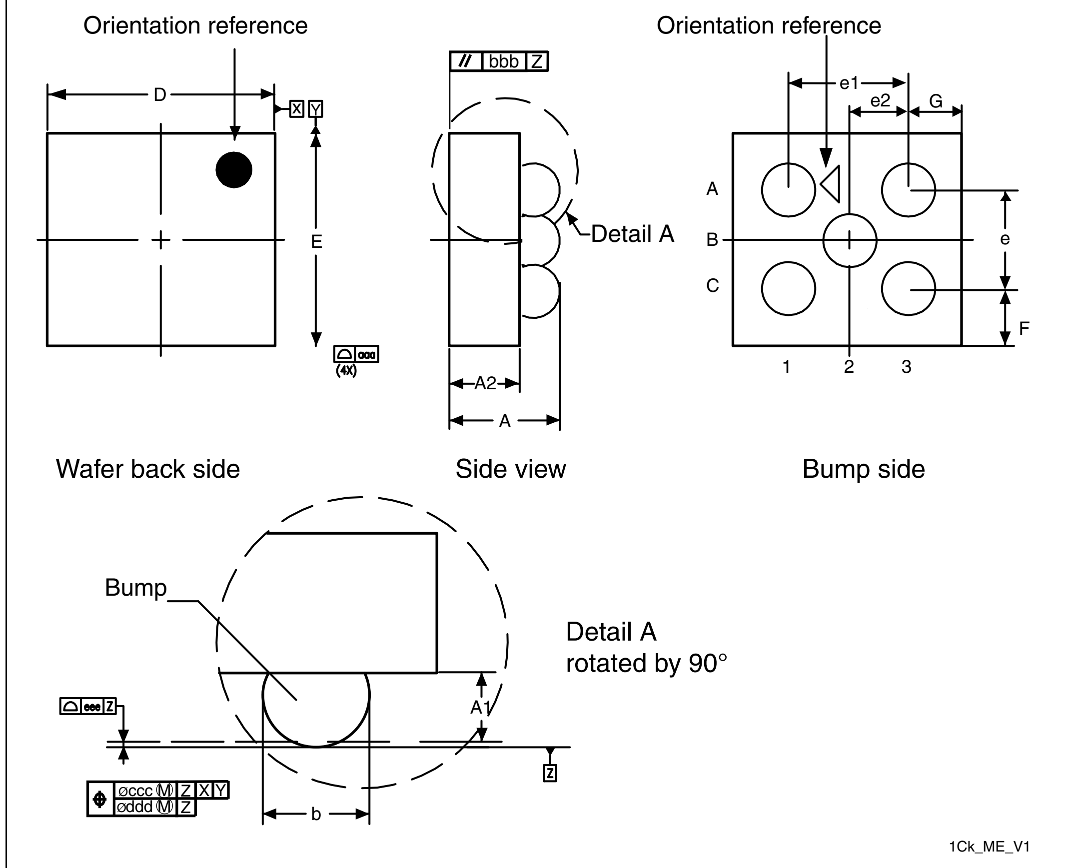
1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is internally pulled to $V_{SS}$. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

**Table 19. UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | 0.550 | 0.450 | 0.600 | 0.0217 | 0.0177 | 0.0236 |
| A1 | 0.020 | 0.000 | 0.050 | 0.0008 | 0.0000 | 0.0020 |
| b | 0.250 | 0.200 | 0.300 | 0.0098 | 0.0079 | 0.0118 |
| D | 2.000 | 1.900 | 2.100 | 0.0787 | 0.0748 | 0.0827 |
| D2 (rev MC) | | 1.200 | 1.600 | | 0.0472 | 0.0630 |
| E | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| E2 (rev MC) | | 1.200 | 1.600 | | 0.0472 | 0.0630 |
| e | 0.500 | | | 0.0197 | | |
| K (rev MC) | | 0.300 | | | 0.0118 | |
| L | | 0.300 | 0.500 | | 0.0118 | 0.0197 |
| L1 | | | 0.150 | | | 0.0059 |
| L3 | | 0.300 | | | 0.0118 | |
| eee[2] | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

**Figure 17. 5-bump WLCSP package outline**



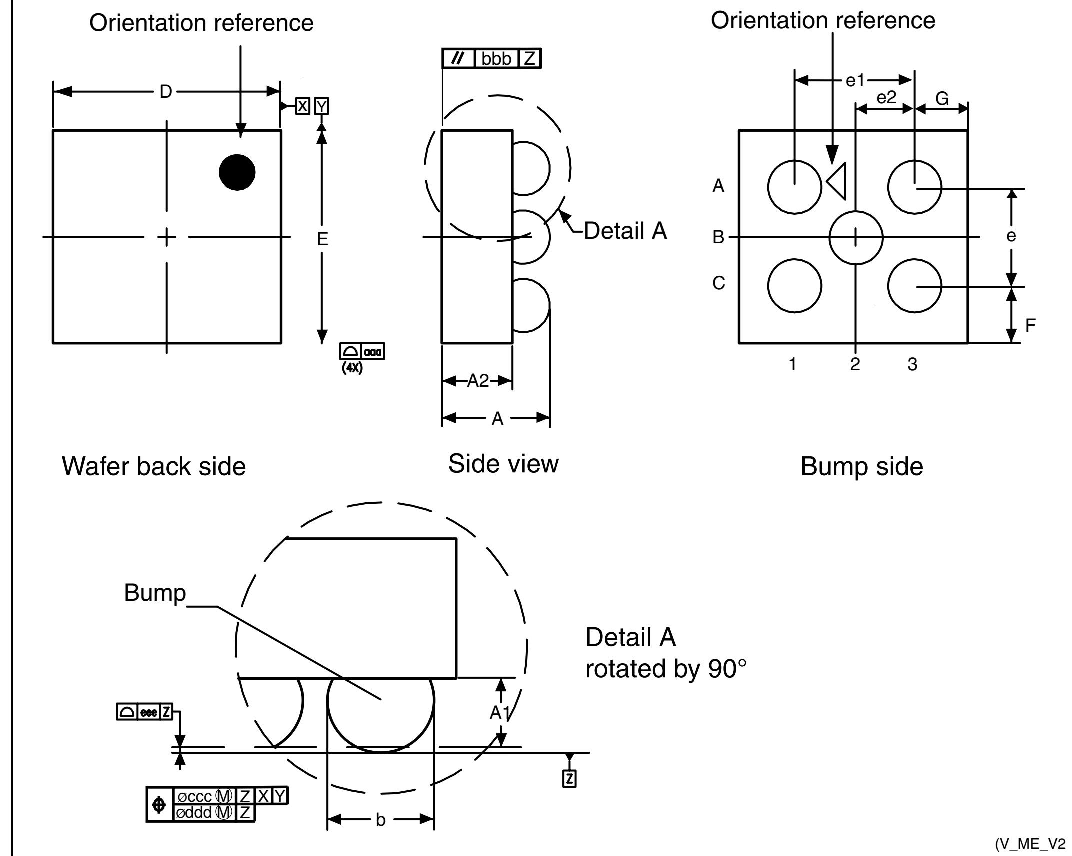

1. Drawing is not to scale.

**Table 20. 5-bump WLCSP package data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | 0.545 | 0.490 | 0.600 | 0.0215 | 0.0192 | 0.0236 |
| A1 | 0.190 | - | - | 0.0075 | - | - |
| A2 | 0.355 | - | - | 0.0140 | - | - |
| b | 0.270 | - | - | 0.0106 | - | - |
| D | 1.215 | - | 1.340 | 0.0478 | | 0.0528 |
| E | 1.025 | - | 1.150 | 0.0404 | - | 0.0453 |
| e | 0.400 | - | - | 0.0157 | - | - |
| e1 | 0.693 | - | - | 0.0273 | - | - |
| e2 | 0.346 | - | - | 0.0136 | - | - |
| F | 0.313 | - | - | 0.0123 | - | - |
| G | 0.261 | - | - | 0.0103 | - | - |
| N (number of terminals) | 5 | | | | | |
| aaa | 0.110 | - | - | 0.0043 | - | - |
| bbb | 0.110 | - | - | 0.0043 | - | - |
| ccc | 0.110 | - | - | 0.0043 | - | - |
| ddd | 0.060 | - | - | 0.0024 | - | - |
| eee | 0.060 | - | - | 0.0024 | - | - |

1. Values in inches are converted from mm and rounded to four decimal digits.

**Figure 18. Thin 5-bump WLCSP package outline**




1. Drawing is not to scale.

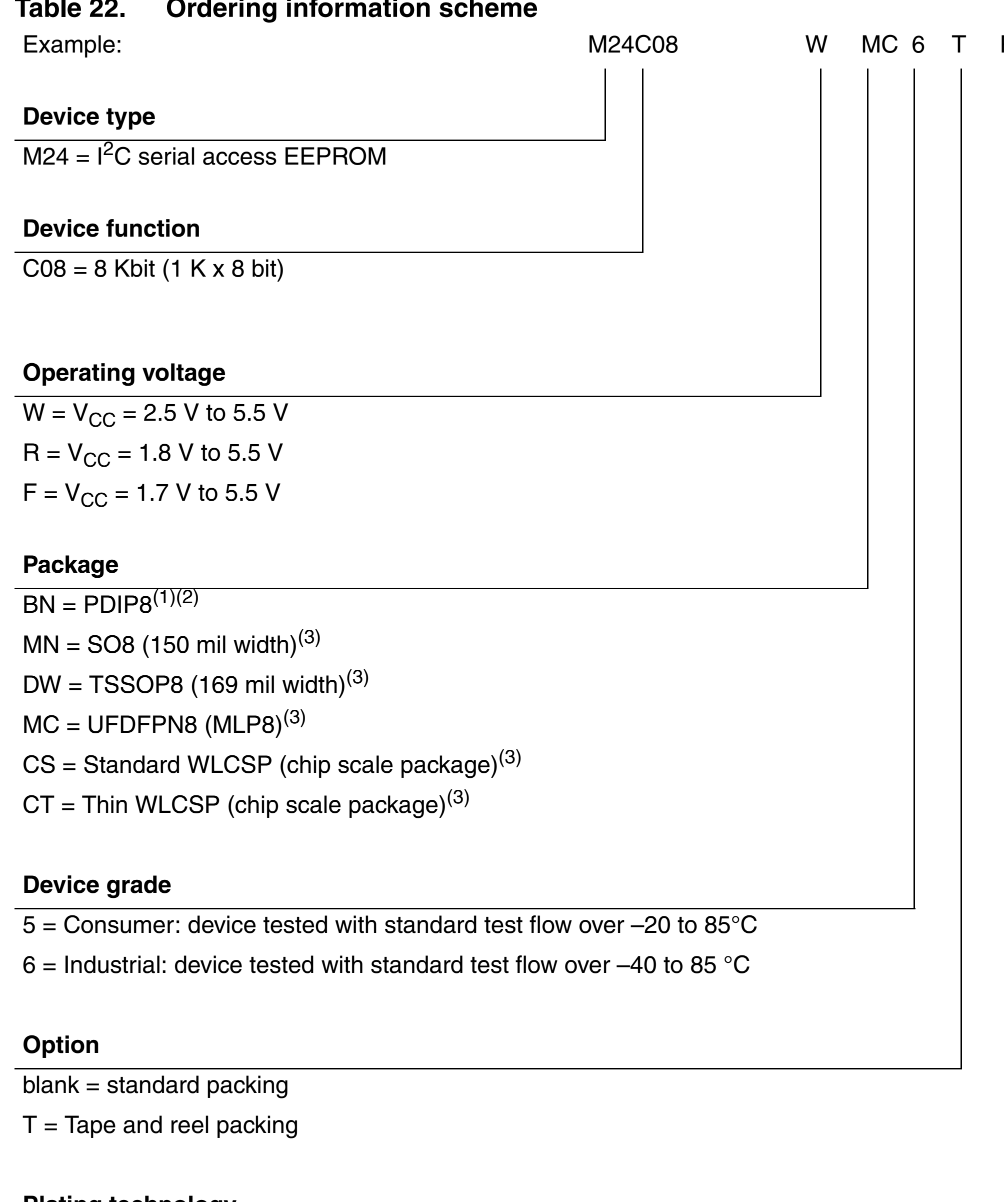
**Table 21. Thin 5-bump WLCSP package data**

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | 0.300 | 0.270 | 0.330 | 0.0118 | 0.0106 | 0.0130 |
| A1 | 0.100 | - | | 0.0039 | | |
| A2 | 0.200 | - | | 0.0079 | | |
| b | 0.160 | - | | 0.0063 | | |
| D | 1.215 | - | 1.340 | 0.0478 | | 0.0528 |
| E | 1.025 | - | 1.150 | 0.0404 | | 0.0453 |
| e | 0.400 | - | - | 0.0157 | | |
| e1 | 0.693 | - | - | 0.0273 | | |
| e2 | 0.346 | - | - | 0.0136 | | |
| F | 0.313 | - | - | 0.0123 | | |
| G | 0.261 | - | - | 0.0103 | | |
| N | 5 | | | | | |
| aaa | 0.110 | - | - | 0.0043 | - | - |
| bbb | 0.110 | - | - | 0.0043 | - | - |
| ccc | 0.110 | - | - | 0.0043 | - | - |
| ddd | 0.060 | - | - | 0.0024 | - | - |
| eee | 0.060 | - | - | 0.0024 | - | - |

1. Values in inches are converted from mm and rounded to four decimal digits.

# 10 Part numbering

**Table 22. Ordering information scheme**




1. RoHS-compliant (ECOPACK1®)
2. Not recommended for new designs.
3. RoHS-compliant and halogen-free (ECOPACK2®)

# 11 Revision history

**Table 23. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 17-Dec-2012 | 1 | New single product M24C08 datasheet resulting from splitting the previous datasheet M24C08-x M24C04-x M24C02-x M24C01-x (revision 18) into separate datasheets. |

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## Document Revision History

| Date | Rev. | Description of the Revision |
|---|---|---|
| June 28, 2013 | 1.00 | First draft creation |
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## Source Documents & Reference Documents

| **Source document Title** | **Rev.:** | **Date:** |
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